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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,552	01/17/2002	Mark S. Styduhar	BUR920010094	8934

28211 7590 07/17/2003

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EXAMINER

NGUYEN, HIEP

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/683,552

Applicant(s)

STYDUHAR, MARK S.

Examiner

Hiep Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: in pages 9-13, it is not clear as to the “notation” ($I^{1/4}s$) is microsecond or something else.

In pages 12 and 13, it not clear how the “analog cycle” (0μ - 31μ) can be overlapped with the “digital cycle” (5μ - 30μ). The Applicant is requested to explain more clearly how these two cycles can be happened. Figure 7 of the present application shows the relationship between the input signal and the output signal. The input is an analog signal and the output is a digital signal. When the input voltage (“analog cycle”) crosses the threshold voltage, the output voltage changes state to a digital signal (“digital cycle”). There is no cycling function of the circuit between the analog configuration and the digital configuration.

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “analog circuit” and “digital circuit” in claims 2, 3, 5, 10, 12, 14, 16, 17, 18, 19, 20, “a first portion”, “a second portion” in claim 16, “an input signal source”, “an output signal source”, “an external input signal source” in claims 17 and 18 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 2, the recitation “said comparator cycles between an analog circuit and a digital circuit” is indefinite because it is unclear what “cycles” is meant by. Figure 7 of the present application shows the relationship between the input signal and the output signal. The input is an analog signal and the output is a digital signal. When the input voltage (analog) crosses a trip threshold voltage, the output voltage changes state. There is no cycling action between an analog circuit and a digital circuit or in other word; the circuit of the present application cannot be both an analog circuit and a digital circuit. The same analysis is true for claims 10 and 16.

Regarding claims 2, 3, 5, 10, 12, 14, 16, 17, 18, 19 and 20; the recitations “analog circuit” and “digital circuit” are indefinite because they are misdescriptive. There are no distinct analog and digital circuits in the drawings of the present application or any possibility of switching from analog state to digital state of the circuit. Figure 7 of the present application shows that the input to the comparator is an analog signal and the output of the comparator is a digital signal. When the analog input signal crosses a threshold voltage, the output changes state and the output signal is a digital signal (basic performance of a comparator).

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, 7-11, 14, and 16-18, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Thiel (US Pat. 5,808,496).

Regarding claim 1, figure 1 of Thiel shows a comparator comprising: a circuit for setting a trip point of a rising edge of an input signal according to a value of an external voltage

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reference (V_{in-}); and at least two transistors (22, 24, 30), in said circuit, for setting a trip point of a falling edge of said input signal according to a width-to-length ratio of said at least two transistors (see col. 3 and 4).

Regarding claim 2, said comparator “cycles” between “an analog circuit” and a “digital circuit”. Note that if the input signal to the comparator is an analog signal and when the input voltage crosses a threshold voltage (trip points) of the comparator, the output changes state and the output is a digital signal.

Regarding claim 5, the input signal (V_{in+}) is greater than the external reference voltage (V_{in-}). Note that (V_{in-}) can be any fixed negative voltage or ground.

Regarding claims 7-9, the least two comparators have transistor lengths and transistor widths and the switching threshold of the falling (descending) edge of the input signal depends on the W/L ratio (col. 3-4).

Regarding claims 10, 11 and 14, figure 1 of Thiel shows a comparator comprising: a circuit (22, 24, 30) for setting a trip point $V(+)$ of a rising (ascending) edge of an input signal (V_{in+}) according to a value of an external voltage reference (V_{in-}); and at least two transistors (22, 30), in said circuit, for setting a trip point of a falling edge of the input signal according to a width-to-length ratio of said at least two transistors, wherein said comparator “cycles” between “an analog circuit” and “a digital circuit”, wherein said trip point of a falling edge of an input signal decreases by decreasing said width-to-length ratio, and wherein said trip point of a falling edge of an input signal increases by increasing said width-to-length ratio (col. 3,4). Note that “cycles” means when the input signal is an analog signal, the output signal will be a digital signal (basic operation of a comparator). The switching threshold depends on the W/L ratio of the transistors (col. 3,4).

Regarding claims 16, 17, 18 and 20, figure 1 of Thiel shows a comparator for controlling a trip point of a rising and falling edge of an external input signal comprising a first portion (30) operatively connected to a second portion (22, 24), wherein said comparator “cycles” between “an analog circuit” and “a digital circuit” (col.3,4). Note that “cycles” means when the input signal is an analog signal, the output signal will be a digital signal (basic operation of a comparator). The tail current source transistor is (30). The first and second pair of transistors are (22, 24) and (26,28). Transistors (38) and (42) act as inverters because they invert the level of

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the input signals applied to their gates. The current mirror load transistor is (26). The input signal $V_{in}(+)$ is greater than the external reference voltage $V_{in}(-)$.

Allowable Subject Matter

Claims 3, 4, 6, 12, 13, 15 and 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 3, 4, 6, 12, 13, 15 and 19 would be allowed because the prior art of record fails to teach or fairly suggest a comparator wherein the rise of the input signal switches the tail current source transistor as called for in claims 3, 12 and 19, a comparator having a plurality of transmission gates and the rise of the input signal causes the comparator to appear as a differential pair in an open loop configuration as called for in claims 4 and 13, as an asymmetric inverting Schmitt trigger as called for in claims 6 and 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen

07-07-03



TUAN T. LAM
PRIMARY EXAMINER